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09/686,259	10/11/2000	Yogesh B. Gianchandani	032026:0485	7008

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EXAMINER	
GOUDREAU, GEORGE A	
ART UNIT	PAPER NUMBER
1763	8

DATE MAILED: 05/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09-686,259	Ganchandani et al.
Examiner	**Group Art Unit**
George Goudreau	1763

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

☒ Responsive to communication(s) filed on (10-001 to 2-031)(i.e., papers #1-7)

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-62 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☒ Claim(s) 23-32, 40-57 is/are allowed.

☒ Claim(s) 1-11, 16, 18, 21-22, 33-39, 58-62 is/are rejected.

☒ Claim(s) 12-15, 17, 19-20 is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement

Application Papers

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119 (a)-(d).

☐ All ☐ Some* ☐ None of the:

☐ Certified copies of the priority documents have been received.

☐ Certified copies of the priority documents have been received in Application No. _____ .

☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a))

*Certified copies not received: _____ .

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 4-5

☐ Interview Summary, PTO-413

☒ Notice of Reference(s) Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other _____

Office Action Summary

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

17. Claims 1-6, 9-10, 21-22, and 58-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bollinger et. al. (5,688,415).

Bollinger et. al. disclose a method for plasma etching layers of ITO, and amorphous Si (60) on a glass substrate (61) using a patterned photo resist etch mask (62), and a plasma comprised of SF6 gas at a process pressure greater than 1 torr. The etching process is used in the fabrication of flat panel displays. The low damage etching process is conducted using a PACE process in which small portions of the surface of the flat panel display are exposed to the plasma at one time. Once plasma etching has been completed in the portion of the flat panel display exposed to the plasma, the substrate is automatically moved such that another untreated region of

the surface of the flat panel display may then be treated with the plasma etchant. The flat panel display (12) is supported on a grounded electrode (44) which is located underneath a plasma formation chamber (14). The plasma is formed using RF biased electrodes (22). A porous conductive reactive gas diffuser (18) is located at the end of the RF biased electrode (22), and is used to expose the surface of the substrate to the plasma. The RF biased electrodes (22) are spaced (1-3) mm above the surface of the substrate to be treated. RF walls (15) made out of a dielectric layer are used to confine the plasma to a selected region of the surface of the substrate to be treated. This is discussed specifically in columns 2-8; and discussed in general in columns 1-10. This is shown in figures 1-5. Bollinger et. al. fail, however, to specifically disclose the following aspects of applicant's claimed invention:

-the specific conduction of a plasma process in which no arcing occurs;

-the specific plasma etching process parameters which are claimed by the applicant; and

-the specific usage of either a DC or an AC power source to power the electrodes used to form the plasma in the process taught above

It would have been obvious to one skilled in the art to employ a plasma process in which no arcing occurs in the process taught above based upon the following. The reference teaches the conduction of a low damage process. Plasma processes in which no arcing occurs are characterized as being low damage processes in the prior art while plasma processes in which arcing does occur are not characterized as being low damage processes.

It would have been obvious to one skilled in the art to replace the RF power source used to power the electrodes used to form the plasma in the process taught above with any of a variety of other types of power sources such as DC or AC power sources. The usage of DC, and AC power sources to power electrodes used to generate a plasma is conventional or at least well known in the plasma etching arts. (The examiner takes official notice in this regard.) Further, this simply represents the usage of an alternative, and at least equivalent means to power the electrodes used to form the plasma in the process taught above to the specific means which are taught above.

It would have been prima facie obvious to employ any of a variety of different process parameters in the plasma etching process taught above including those which are specifically claimed by the applicant. These are all well known variables in the plasma etching art which are known to effect both the rate and quality of the plasma etching process. Further, the selection of particular values for these variables would not necessitate any undo experimentation which would be indicative of a showing of unexpected results.

Alternatively, it would have been obvious to one skilled in the art to employ the specific etch process parameters which are claimed by the applicant in the etching process taught above based upon In re Aller as cited below.

"Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F. 2d 454, 105 USPQ 233, 235 (CCPA).

Further, all of the specific process parameters which are claimed by the applicant are results effective variables whose values are known to effect both the rate, and the quality of the plasma etching process.

18. Claims 1-2, 4-11, 21-22, 33-34, 36-39, and 58-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zarowin et. al. (5,811,021).

Zarowin et. al. disclose a process, and apparatus for plasma etching or plasma CVD depositing a coating onto the surface of a Si wafer. The process is characterized as a low damage process. The etching process may be conducted in a plasma comprised of Cl2 at a process pressure between (1-10) torr. The deposition process may be conducted in a plasma comprised of SiCl4. The deposition or etching process may be conducted on a selected portion of the wafer surface by moving an RF biased electrode (32) over the surface of the wafer. The wafer rests on an RF biased cathode (i.e.-plate). This is discussed specifically in columns 4-5, 10, 15; and discussed in general in columns 1-22. This is shown in figures 1-12. Zarowin et. al. fail, however, to specifically disclose the following aspects of applicant's claimed invention:

-the specific conduction of a plasma process in which no arcing occurs;

-the specific plasma etching process parameters which are claimed by the applicant; and

-the specific usage of either a DC or an AC power source to power the electrodes used to form the plasma in the process taught above

It would have been obvious to one skilled in the art to employ a plasma process in which no arcing occurs in the process taught above based upon the following. The reference teaches the

conduction of a low damage process. Plasma processes in which no arcing occurs are characterized as being low damage processes in the prior art while plasma processes in which arcing does occur are not characterized as being low damage processes.

It would have been obvious to one skilled in the art to replace the RF power source used to power the electrodes used to form the plasma in the process taught above with any of a variety of other types of power sources such as DC or AC power sources. The usage of DC, and AC power sources to power electrodes used to generate a plasma is conventional or at least well known in the plasma etching arts. (The examiner takes official notice in this regard.) Further, this simply represents the usage of an alternative, and at least equivalent means to power the electrodes used to form the plasma in the process taught above to the specific means which are taught above.

It would have been prima facie obvious to employ any of a variety of different process parameters in the plasma etching process taught above including those which are specifically claimed by the applicant. These are all well known variables in the plasma etching art which are known to effect both the rate and quality of the plasma etching process. Further, the selection of particular values for these variables would not necessitate any undo experimentation which would be indicative of a showing of unexpected results.

Alternatively, it would have been obvious to one skilled in the art to employ the specific etch process parameters which are claimed by the applicant in the etching process taught above based upon In re Aller as cited above. Further, all of the specific process parameters which are

claimed by the applicant are results effective variables whose values are known to effect both the rate, and the quality of the plasma etching process.

19. Claims 1-6, 8-11, 16, 21-22, 33-39, and 58-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakakibara et. al. (5,397,420).

Sakakibara et. al.

Sakakibara et. al. disclose an apparatus, and process for plasma etching a pattern in a Si wafer using an RF biased electrode (21) which is rastered across the face of the wafer to form a pattern in the Si. The wafer rest on an RF biased cathode (i.e.-plate). Alternatively, the wafer may rest on a grounded cathode (i.e.-plate). They employ a plasma comprised of HBr to conduct their low damage etching process. The RF biased electrode is located several mms. above the surface of the Si wafer to be etched during the etching process. This is discussed specifically in columns 4-7; and discussed in general in columns 1-10. This is shown in figures 1-11. Sakakibara et. al. fail, however, to specifically disclose the following aspects of applicant's claimed invention:

-the specific usage of a plasma etchant which is comprised of SF6 to etch the Si;

-the specific conduction of a plasma process in which no arcing occurs;

-the specific plasma etching process parameters which are claimed by the applicant; and

-the specific usage of either a DC or an AC power source to power the electrodes used to form the plasma in the process taught above

It would have been obvious to one skilled in the art to etch the Si wafer using a plasma etchant which is comprised of SF6 in the process taught above based upon the following. The usage of a plasma which is comprised of SF6 to etch a Si wafer is conventional or at least well known in the plasma etching arts. (The examiner takes official notice in this regard.) Further, this simply represents the usage of an alternative, and at least equivalent means for etching the Si wafer in the process taught above to the specific means which are taught above.

It would have been obvious to one skilled in the art to employ a plasma process in which no arcing occurs in the process taught above based upon the following. The reference teaches the conduction of a low damage process. Plasma processes in which no arcing occurs are characterized as being low damage processes in the prior art while plasma processes in which arcing does occur are not characterized as being low damage processes.

It would have been obvious to one skilled in the art to replace the RF power source used to power the electrodes used to form the plasma in the process taught above with any of a variety of other types of power sources such as DC or AC power sources. The usage of DC, and AC power sources to power electrodes used to generate a plasma is conventional or at least well known in the plasma etching arts. (The examiner takes official notice in this regard.) Further, this simply represents the usage of an alternative, and at least equivalent means to power the electrodes used to form the plasma in the process taught above to the specific means which are taught above.

It would have been prima facie obvious to employ any of a variety of different process parameters in the plasma etching process taught above including those which are specifically claimed by the applicant. These are all well known variables in the plasma etching art which are known to effect both the rate and quality of the plasma etching process. Further, the selection of particular values for these variables would not necessitate any undo experimentation which would be indicative of a showing of unexpected results.

Alternatively, it would have been obvious to one skilled in the art to employ the specific etch process parameters which are claimed by the applicant in the etching process taught above based upon In re Aller as cited above. Further, all of the specific process parameters which are claimed by the applicant are results effective variables whose values are known to effect both the rate, and the quality of the plasma etching process.

20. Claims 18, 60-61 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

-The wording used in claim 18 is very confusing, and should be reworded.; and

-Claims 60, and 61 incorrectly claim the same subject matter. (These claims are duplicative of each other.)

21. Claims 12-15, 17, and 19-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

22. Claims 23-32, and 40-57 are allowed.

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner George A. Goudreau whose telephone number is (703) -308-1915. The examiner can normally be reached on Monday through Friday from 9:30 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Examiner Gregory Mills, can be reached on (703) -308-1633. The appropriate fax phone number for the organization where this application or proceeding is assigned is (703) -306-3186.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) -308-0661.

George A. Goudreau/gag

Primary Examiner

AU 1763